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Using the New (Rev 1) PowerPC 604 Hardware Specification

Application Note AN-PPC-006

Use the new 604 hardware specification to optimize CPU selection and system timing.

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Tim Saunders
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1 New 604 Hardware Specification Format

In the new *PowerPC 604 RISC Microprocessor Hardware Specification* (MPR604HSU-02) the AC timings are specified as a function of the speed grade of the 604, which is expressed in terms of the maximum internal CPU clock frequency. The AC timings are independent of the frequency of the SYSCLK input and the CPU and VCO frequencies. The new hardware spec gives the AC timings for three speed grades of the 604: 100 MHz, 120 MHz, and 133 MHz.

This application note describes how to use the hardware specification to choose the CPU speed grade and optimize the system timing.

2 The 604 Clock PLL

2.1 PLL Hardware

As shown in Figure 1, the 604 uses a phase-locked loop (PLL) to generate the internal clock (CPU clock), using the bus clock (SYSCLK) as a reference. The voltage controlled oscillator (VCO) generates a signal that is either 2x or 4x the CPU clock frequency. The VCO frequency is divided down by the VCO:CPU clock divider. The CPU clock is then divided down by the CPU:SYS clock divider and phase compared to SYSCLK. The resulting error voltage is used to correct the frequency of the VCO so as to phase lock it to SYSCLK.

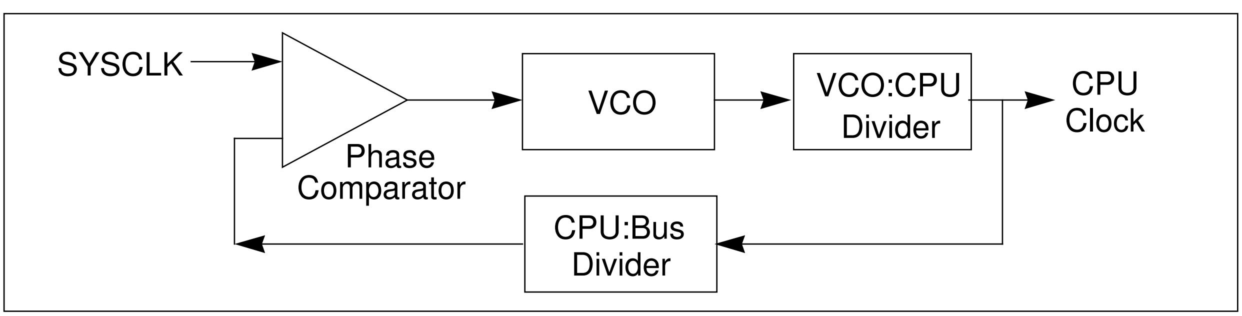

Figure 1. Conceptual Model of 604 Clock PLL

2.2 PLL Configuration

The VCO:CPU clock divider is controlled by PLL_CFG[2:3] such that:

PLL_CFG[2:3]	VCO:CPU
00	2:1
01	4:1

The CPU:Bus clock divider is controlled by PLL_CFG[0:1] such that:

PLL_CFG[0:1]	Divide By
00	1:1
01	2:1
10	3:1
11	3:2

As shown in Table 12 of the hardware spec, not all possible combinations of PLL_CFG[0:3] are allowed. The selected configuration must keep the VCO and CPU clocks within the recommended operating conditions shown in Table 5 of the hardware spec.

2.3 Recommended Operating Conditions

2.3.1 Clock and AC Specifications

The first two rows of Table 5 of the hardware spec limit the frequency at which the 604 clocks can be operated. The top row, Frequency of operation, shows the frequency range over which the CPU clock will operate reliably for the three different speed grades. The second row, Frequency of VCO, shows the frequency range over which the VCO will operate reliably. These two specifications must be complied with for proper system operation. Likewise, the rise and fall time, duty cycle, and jitter must be compliant.

The third row of Table 5 of the hardware spec, SYSCLK frequency, merely shows the range over which the SYSCLK is tested. The 604 will operate correctly with faster SYSCLK operation as long as the CPU clock and VCO frequencies are compliant, and all of the bus timings (setup, hold, enable, disable, &etc.) requirements are met.

2.3.1 Typical PLL Configurations

Table 12 of the hardware spec shows some recommended settings of the CPU and (VCO) frequencies for given SYSCLK frequencies. This table replaces the one shown in the 604 User’s Manual. For each of the PLL configurations listed in the left-most column, the table lists several valid combinations of SYSCLK, CPU clock, and VCO operating frequencies. Note that other frequency choices are also available. For example, in the first row of the table, an example is given for 50MHz and 60MHz SYSCLK operation, but the 604 can also be run with SYSCLK = 55MHz using the same PLL configuration.

2.4 Putting it All Together

The objective is to maximize system performance using the available resources. Table A summarizes the following three examples, which illustrate the use of Tables 5 and 12 of the hardware spec.

Table A. Summary of Examples

System Specification	Example 1	Example 2	Example 3	Units
VCO frequency	240	266	240	Mhz
VCO:CPU ratio	2:1	2:1	3:2	
CPU Clock frequency	120	133	120	MHz
CPU:SYSCLK ratio	2:1	2:1	3:2	
SYSCLK Frequency	60	66	80	MHz
PLL_CFG(0-3)	0100	0100	1100	

2.4.1 240:120:60

Suppose that initial system considerations call for the 604 to operate at 120MHz, with a bus speed of less than or equal to 66MHz. Hardware spec Table 5 shows that both the 120MHz and the 133MHz speed grades will work, because the required CPU clock and VCO frequencies are within the recommended operating range. Hardware spec Table 12 shows that 60MHz bus operation can be achieved using a 2:1 CPU:Bus clock ratio, and a 2:1 VCO:CPU clock ratio, resulting in 240:120:60MHz VCO:CPU:Bus operation.

2.4.2 266:133:66

Suppose that 240:120:60MHz operation does not yield fast enough bus operation. One solution would be to upgrade the design to the 133MHz 604. Hardware spec Table 12 shows a valid combination at 266:133:66.

2.4.3 240:120:80

Suppose that a bus speed faster than 60MHz is desired for a system using the 120MHz 604. As far as the 604 is concerned, it is valid to operate the 120MHz 604 at 240:120:80, but a system timing analysis is required to determine if the 604 will satisfy the system timing requirements at that bus speed.

To construct a simple example, suppose that the system contains a 604 that is only connected to one other device, which has a bus interface whose timing is identical to that of the 604. Tables 5, 6, and 7 of the hardware spec then show the timing of both devices. It is good practice to analyse the timing of each signal net for each different switching scenario. This example will only consider the timing of a TS# assertion.

Based on the chosen SYSCLK frequency of 80 MHz, the designer has a total bus clock cycle time of 12.5ns to accommodate inputs, outputs, and any system overhead. Line 13b of Table 7 of the hardware spec shows that the maximum output valid delay time for TS# is 6.5ns for a 3.6v bus. Line 7 of Table 6 shows that the minimum input setup time is 5ns. Thus device timing requires a total of 11.5ns, leaving 12.5ns minus 11.5ns equals 1 ns for system overhead, such as flight time, settling time, and clock skew.

If the system requires more than 1ns for overhead, then the designer can either reduce the bus clock frequency (to increase the bus cycle period), or select a higher speed 604. Upgrading the design to the 133MHz 604 reduces the output valid delay from 6.5ns to 6ns, which increases the allowable system overhead from 1ns to 1.5ns.

3 Summary

The AC Timing specifications of the 604 are now characterized by CPU speed sort. System designers can choose a higher speed 604 to meet tighter system and bus design constraints at higher bus clock speeds, or choose a slower speed CPU to reduce the cost of systems running at slower speeds. This allows the designer to optimize the system for CPU cost and system performance.

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USA and Canada:
IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) PowerFax
http://www.chips.ibm.com/products/ppc
http://www.ibm.com
ftp://ftp.austin.ibm.com/pub/PPC_support

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